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09/960,495	09/24/2001	Hiroyuki Amishiro	50090-338	5812

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EXAMINER	
HOGANS, DAVID L	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/960,495	AMISHIRO ET AL.	
	Examiner	Art Unit	
	David L. Hogans	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 21* is/are pending in the application.

4a) Of the above claim(s) *14-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9,11 and 13* is/are rejected.

7)☒ Claim(s) *6-8,10,12 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on February 27, 2004.

Status of Claims

Claims 1-13 and 21 are pending. Claims 14-20 are withdrawn.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "dummy gate electrodes 7" at page 21 line 23 of Applicant's specification. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

The objection of Claim 9 under 37 C.F.R. 1.75(c) is withdrawn pursuant to Applicant's comments filed on February 27, 2004.

Claim Rejections - 35 USC § 112

The rejection of Claims 1-3, 11 and 13 via 35 U.S.C. § 112, first paragraph, are withdrawn pursuant to Applicant's comments filed on February 27, 2004.

The rejection of Claims 1-13 and 21 via 35 U.S.C. § 112, second paragraph, concerning uncertainty as to if the plurality of resistor elements are formed on a single insulation film, are withdrawn pursuant to Applicant's comments filed on February 27, 2004.

The rejection of Claims 1-13 and 21 via 35 U.S.C. § 112, second paragraph, concerning the phrase "predetermined", are withdrawn pursuant to Applicant's comments filed on February 27, 2004.

The rejection of Claims 1-3, 9-11, 13 and 21 via 35 U.S.C. § 112, second paragraph, are withdrawn pursuant to Applicant's comments filed on February 27, 2004.

The rejection of Claim 4 via 35 U.S.C. § 112, second paragraph, is withdrawn pursuant to Applicant's comments filed on February 27, 2004.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 5 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by US 2002/0033519 to Babcock et al.

In reference to Claims 5 and 9, Babcock et al. teaches:

- active regions (80) proximate to each of the resistor elements (60 and 70) (See paragraphs 0017-0021 and Figures 2A-2D)
- the regions including the active regions are furnished with dummy gate electrodes (80) constituting the same layer as that of said resistor elements (See paragraphs 0017-0021 and Figures 2A-2D)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 2002/0033519 to Babcock et al. in view of Silicon Processing for the VLSI Era (2000), Volume 1, to Wolf et al.

Claim 1

Babcock et al., in paragraphs 0017-0021 and Figures 2A-2D, teaches a plurality of resistor elements (60 and 70) formed on an element isolating insulating film (20) in predetermined regions and active regions (80) proximate to each of said resistor elements (60 and 70), wherein said active regions are formed in said semiconductor substrate. Furthermore, Babcock et al. teaches plural isolation structures, CMOS circuits and transistor gate structures.

Babcock et al. fails to explicitly teach wherein the active regions partition the element isolating insulating film between adjacent resistor elements.

However, Wolf et al., on page 301, teaches that MOS devices (i.e. – active regions) are isolated from each other by shallow trench isolation structures.

It would have been obvious to one of ordinary skill in the art to modify Babcock et al. by incorporating active regions on either side of an insulating region, as taught by Wolf et al., to isolate adjacent active regions, thereby preventing coupling.

Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to place another active region/resistor element combination adjacent the previous active region/resistor element combination to create an array of programmable structures, since it has been held that mere duplication of the essential working parts has no patentable significance unless a new and unexpected result is produced. *In re Harza*, 274 F.2d 669 (CCPA 1960)

Claim 2

Incorporating all arguments of Claim 1 and noting that Babcock et al., in paragraphs 0017-0021 and Figures 2A-2D, teaches an insulating film (20) formed by STI. Furthermore, the Examiner notes that the patentability of a product does not

depend on its method of production. Therefore, the limitation that the insulating film is formed by shallow trench isolation carries no patentable weight.

"Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not. Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Claim 3

Incorporating all arguments of Claim 1 and noting that Babcock et al., in paragraphs 0017-0021 and Figures 2A-2D, teaches wherein said insulating film (20) is set to a predetermined width by said active regions (80).

Claim 11

Incorporating all arguments of Claim 1 and noting that Babcock et al., in paragraphs 0017-0021 and Figures 2A-2D, teaches wherein said active regions (80) extend close to lengthwise ends of said resistor elements (60 and 70).

Claim 13

Incorporating all arguments of Claim 1 and noting that Babcock et al., in paragraphs 0017-0021 and Figures 2A-2D, teaches wherein said resistor elements (60 and 70) are formed by a layer constituting gate electrodes of MOS transistors (80) outside said predetermined regions.

5. Claims 1-3 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 2002/0084886 to Wu. in view of US 2002/0033519 to Babcock et al.

Claim 1

Wu, in Figures 2A-2G and paragraphs 0025-0034, teaches a resistor element (214) formed on an element isolating insulating film (202) in predetermined regions and active regions (220) proximate to each of said resistor element, wherein said active

region is formed in said semiconductor substrate and partition said element isolating insulating film. Furthermore, Wu teaches that the isolating region (202) separates the active regions. (See Figure 2 and page 2 paragraph 0025)

Wu fails to explicitly teach a plurality of resistor elements formed on an element isolating insulating film.

However, Babcock et al., in paragraphs 0017-0021 and Figures 2A-2D, teaches a plurality of resistor elements (60 and 70) formed on an insulating film (20).

It would have been obvious to one of ordinary skill in the art to modify Wu by incorporating a plurality of resistor elements formed on an insulating film, as taught by Babcock et al., to provide heating elements adjacent to a resistor or fuse that can greatly reduce the current needed to trim the resistor or program the fuse.

Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to place another active region/resistor element combination adjacent the previous active region/resistor element combination to create a high resistance transistor gate array, since it has been held that mere duplication of the essential working parts has no patentable significance unless a new and unexpected result is produced. *In re Harza*, 274 F.2d 669 (CCPA 1960)

Claim 2

Incorporating all arguments of Claim 1 and noting that Wu, in Figures 2A-2G and paragraphs 0025-0034 teaches an insulating film (202) formed by STI. The Examiner notes that the patentability of a product does not depend on its method of production. Therefore, the limitation that the insulating film is formed by shallow trench isolation carries no patentable weight.

"Even though product -by[-] process claims are limited by and defined by the process, determination of patentability is based upon the product itself. The patentability of a product does not depend on its method of production. If the product in product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product is made by a different process." *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985)(citations omitted).

A *"product by process"* claim is directed to the product per se, no matter how actually made, *In re Hirao and Sato et al.*, 190 USPQ 15 at 17 (CCPA 1976) (footnote 3). See also *In re Brown and Saffer*, 173 USPQ 685 (CCPA 1972): *In re Luck and Gainer*, 177 USPQ 523 (CCPA 1973); In re Fessmann, 180 USPQ 324 (CCPA 1974); and *In re Marosi et al.*, 218 USPQ 289 (CAFC 1983) final product per se which must be determined in a *"product by, all of"* claim, and not the patentability of the process, and that an old or obvious product, whether claimed in *"product by process"* claims or not.

Note that Applicant has the burden of proof in such cases, as the above caselaw makes clear.

Claim 3

Incorporating all arguments of Claim 1 and noting that Wu, in Figures 2A-2G and paragraphs 0025-0034, teaches wherein said insulating film (202) is set to a predetermined width by said active regions (220).

Claim 11

Incorporating all arguments of Claim 1 and noting that Wu, in Figures 2A-2G and paragraphs 0025-0034, teaches wherein said active regions (220) extend close to lengthwise ends of said resistor elements (214).

Response to Arguments

6. Applicant's arguments filed February 27, 2004, have been fully considered but they are not persuasive.

Claims 5 and 9 rejected under 35 U.S.C. 102(e) as being anticipated by US 2002/0033519 to Babcock et al.

Initially, the Applicant proffers that Claims 5 and 9 are not taught by US 2002/0033519 to Babcock et al. under 35 U.S.C. 102(e). The Applicant states: "Applicants are unable to determine where Babcock teaches or suggest that active

regions 80 are proximate to each of the resistor elements 60, 70. Feature 80 is illustrated in Figs. 2B and 2C, but feature 80 is not proximate to each of the resistor elements, as recited in claim 5.". The Examiner notes that Figure 2 of Babcock et al. does teach an active region (80) proximate to each of the resistor elements. As defined by Applicant in their preamble, said resistor elements is a "plurality of resistor elements". Therefore, since each resistor element is a plurality of resistor elements, the active region (80) of Babcock et al. is proximate to each resistor element. Furthermore, since Wolf et al. teaches isolating adjacent MOSFETs with STI structures, it would have been obvious to one of ordinary skill in the art to place a duplicate Babcock et al. structure adjacent to the original Babcock et al. structure, to create an array of programmable structures.

Claims 1-3, 11 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over US 2002/0033519 to Babcock et al. in view of Silicon Processing for the VLSI Era (2000), Volume 1, to Wolf et al.

Next, the Applicant proffers that Claims 1-3, 11 and 13 are not taught by US 2002/0033519 to Babcock et al. in view of Silicon Processing for the VLSI Era (2000), Volume 1, to Wolf et al. Firstly the Applicant suggests that *In re Harza* does not apply because the Examiner did not establish "that the cited case law is relevant to the factual situation of application under examination. If the Examiner did not have this burden, the Examiner could cite any number of cases (i.e., hundreds of cases) for any proposition and place undue hardship upon the Applicant to determine whether or not those cases

actually applied". The Examiner notes that *In re Harza* was not cited for establishing the burden of prima facie obviousness. This element (prima facie obviousness) was satisfied by the Examiner providing the motivation, within the 35 U.S.C. 103 rejection, of "preventing coupling". Additionally, the Examiner notes that MPEP § 2144 does not explicitly place the burden of proof upon the Examiner to prove that the facts in a prior legal decision are sufficiently similar. Further, the Examiner notes that Babcock et al. possesses all of the limitations of the Applicant's claimed invention and that mere replication of the elements would be within the ordinary skill of one within the art to create a programmable gate array.

Secondly, the Applicant argues that a gate structure with a gate oxide layer would not constitute an active region or an active region within a substrate. To this end, the examiner has affixed the rudimentary definitions of an "active region" and a "MOSFET", provided by a dictionary of electronics. It is the Examiner's position that one of ordinary skill in the art would know that an "active region" produces gain and that a "MOSFET" contains active regions within a substrate. Thirdly, the Applicant argues that "the Examiner has failed to establish that one of such active regions would necessarily partition an insulating film between adjacent resistor elements that are each formed on the insulating film, as recited in claim 1.". As this argument mirrors the argument provided by the Applicant under the rejection of Claims 5 and 9 above, the Examiner will summarily address it. Since Applicant defined resistor elements, as a

plurality of resistor elements, the active regions of Babcock et al. separate such plurality of resistor elements.

Of note, is Applicant's acknowledgement that "Babcock already discloses a structure capable of performing an array of programmable structures.". If Applicant concedes that Babcock et al. teaches an array, then it necessarily follows that the active regions (80) would partition adjacent plurality of resistors; as an array is a matrix of these cells placed side by side.

Claims 1-3 and 11 rejected under 35 U.S.C. 103(a) as being unpatentable over US 2002/0084886 to Wu et al. in view of US 2002/0033519 to Babcock et al.

Finally, the Applicant proffers that Claims 1-3 and 11 are not taught by US 2002/0084886 to Wu et al. in view of US 2002/0033519 to Babcock et al. As to the *In re Harza* argument, please see above. Applicant argues that "the Examiner has failed to establish that one of the active region of Wu would necessarily partition an insulating film between adjacent resistor elements that are each formed on the insulating film". As this argument has been repeated twice above, the Examiner will summarily note that since Applicant defined resistor elements, as a plurality of resistor elements, the active regions of Wu separate such plurality of resistor elements in view of Babcock et al.

Allowable Subject Matter

1. Claims 4, 6-8, 10, 12 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

2. The following is a statement of reasons for the indication of allowable subject matter.

With regard to Claim 4, the prior art of record, in combination with the other claimed features, fails to teach wherein said insulating film under said resistor elements is set to a predetermined width by said active regions, wherein said predetermined width is defined by an amount of shift in resistance value of said resistor elements, said amount of shift being defined by said predetermined width.

With regard to Claims 6-8, the prior art of record, in combination with the other claimed features, fails to teach wherein said dummy gate electrodes entirely cover the active regions, or wherein said active regions are covered with a plurality of dummy gate electrodes, or wherein a distance between each of said resistor elements and each of said dummy gate electrodes is held constant.

With regards to Claim 10, the prior art of record, in combination with the other claimed features, fails to explicitly teach wherein the minimum space between any adjacent two of said plurality of said resistor elements is formed by a conductive film constituting the same layer as the resistor elements.

With regards to Claim 12, the prior art of record, in combination with the other claimed features, fails to explicitly teach wherein the resistor elements are surrounded by the dummy gate electrodes.

With regard to Claim 21, the prior art of record, in combination with the other claimed features, fails to explicitly teach wherein the distance between adjacent plurality of resistor elements is approximately equal to the distance between any adjacent pair of resistor elements and the dummy gate electrodes.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 6,340,833 to Liu et al. teaches an active region (16a, 17 and 19) partitioning element isolation regions (12) with a resistive element (16b) formed thereover.

US 6,284,599 to Mehrad et al. teaches an active region (23, 170 and 180) partitioning element isolation regions (70) with a resistive element (16) formed thereover.

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Hogans whose telephone number is (571) 272-1691. The examiner can normally be reached on M-F (7:30-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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